LISTING OF CLAIMS:

The following listing of claims replaces all previous versions and listings in the present application.

1. (Currently amended) A low-pass filter for detecting voltage variations of an input signal supplied to an input terminal thereof and producing and output signal indicative of said voltage variations, said low-pass filter ~~being constituted by~~including a switched capacitor circuit having clock signal generating means for generating a first clock pulse signal and a second clock pulse signal of mutually identical frequency and differing phase, first, second and third capacitors, a first plurality of switching elements each controlled by said first clock pulse signal, and a second plurality of switching elements each controlled by said second clock signal, an operational amplifier for producing said output signal from an output terminal thereof, a first capacitor selectively connectable between said low-pass filter input terminal and an input terminal of said operational amplifier via respective ones of said first and second pluralities of switching elements, a second capacitor selectively connectable between an input terminal of said operational amplifier and said output terminal of said operational amplifier via respective ones of said second plurality of switching elements, a third capacitor connected between said input terminal and output terminal of said operational amplifier,~~with each of said switching elements connected to at least one of said capacitors,~~ said low-pass filter configured to operate successively ~~operating~~ in:

a first condition in which said first clock pulse signal is at an active level whereby each of said first plurality of switching elements is held in a conducting status and said second clock pulse signal is at an inactive level whereby each of said second plurality of switching elements is

held in a non-conducting status, with said first capacitor being thereby charged to a voltage of said input signal, said second capacitor being discharged to a voltage of zero, and no charging or discharging of said third capacitor is performed,

a second condition, in which each of said first clock pulse signal and second clock pulse signal is at said ~~active~~inactive level, whereby no charging or discharging of said first, second or third capacitors is performed,

a third condition in which said first clock pulse signal is at said inactive level and said second clock pulse signal is at said active level, whereby each of said second plurality of switching elements is held in a conducting status and said second and third capacitors thereby become connected in parallel with one another, said first capacitor is discharged to a voltage of zero, and a discharge current from said first capacitor acts to charge said second and third capacitors, and

a fourth condition in which each of said first clock pulse signal and second clock pulse signal is at said inactive level, whereby no charging or discharging of said first, second or third capacitors is performed,

with said first condition being subsequently returned to;

wherein

said clock signal generating circuit comprises means for controlling said first and second pulse signals ~~such that said fixedly predetermined~~to set a duration of each interval of the second condition~~, which elapses~~ at a value whereby a decrease of stored charge in said first capacitor occurring within said interval, expressed as a percentage decrease with respect to an amount of said stored charge at commencement of said interval, is predetermined to be substantially equal to a maximum permissible amount of error of DC gain of said low-pass filter, with said error

being no greater than 3 percent of a predetermined value of said DC gain, said duration extending between a transition of said first clock pulse signal from said active level to said inactive level and an immediately succeeding transition of said second clock pulse signal from said inactive level to said active level~~, is made as short as possible within a range of time interval values whereby none of said first plurality of switching elements are in said conducting status concurrently with any of said second plurality of switching elements~~.

2. (Currently amended) A low-pass filter for detecting voltage variations of an input signal applied between first and second input terminals thereof and producing an output signal indicative of said voltage variations, ~~configured as~~said low pass filter including a switched capacitor circuit having first and second input terminals coupled to receive said input signal, a clock signal generating circuit for generating a first clock pulse signal and a second clock pulse signal of mutually identical frequency and differing phase, first, second and third capacitors, a set of first, second and third switching elements each controlled to be set in a conducting status when said first clock pulse signal is at an active level, a set of fourth, fifth and sixth switching elements each controlled to be set in said conducting status when said second clock pulse signal is at said active level, an operational amplifier which operates from a single power supply voltage and has an inverting input terminal thereof connected in common to a reference voltage having a value that is one-half of said power supply voltage and to said second input terminal of said switched capacitor circuit, said first switching element connected between said first input terminal of said switched capacitor circuit and a first mutual connection node, said fourth switching element connected between said first mutual connection node and a non-inverting input terminal of said operational amplifier, said first capacitor connected between said first mutual connection node and a second mutual connection node, said second switching element

connected between said second mutual connection node and said non-inverting input terminal of said operational amplifier, said fifth switching element connected between said second mutual connection node and said inverting input terminal of said operational amplifier, said second capacitor connected between said second mutual connection node and a third mutual connection node, said third capacitor connected between said inverting input terminal of said operational amplifier and an output terminal of said operational amplifier, said third switching element connected between said third mutual connection node and said non-inverting input terminal of said operational amplifier, said sixth switching element connected between said third mutual connection node and said output terminal of said operational amplifier, with ~~an~~said output signal of said low-pass filter being produced between said output terminal of said operational amplifier and said non-inverting input terminal of said operational amplifier; wherein

said clock signal generating circuit comprises means for generating said first clock signal and said second clock signal such that a ~~time~~duration of an interval which elapses between a transition of said first clock signal from said active level to an inactive level and an immediately succeeding transition of said second clock signal from said inactive level to said active level is ~~made as short as possible within a range of values whereby none of said of first, second and third switching elements can enter said conducting status concurrently with any of said fourth, fifth and sixth switching elements~~set at a value whereby a decrease of stored charge in said first capacitor occurring within said interval, expressed as a percentage decrease with respect to an amount of said stored charge at commencement of said interval, is predetermined to be substantially equal to a maximum permissible amount of error of DC gain of said low-pass filter, with said error being not greater than 3 percent of a predetermined value of said DC gain.

3. (Currently amended) A low-pass filter as claimed in claim 1, wherein said switching elements are ~~semiconductor devices~~field effect transistors which exhibit leakage current flow, and wherein said duration of the second condition is made as short as possible within a range of values whereby none of said of first, second and third ~~switching elements~~field effect transistors can enter said conducting status concurrently with any of said fourth, fifth and sixth ~~switching elements~~field effect transistors while said low-pass filter is functioning at a predetermined maximum operating temperature thereof.

4. (Original) A low-pass filter as claimed in claim 1, wherein said duration of the second condition is set as a value within a range extending from 0.6 microseconds to 2 microseconds.

5. (Canceled)

6. (Currently amended) A low-pass filter ~~configured as~~including a switched capacitor circuit, for detecting voltage variations of an input signal and producing an output signal indicative of said voltage variations, ~~including~~ comprising:

first and second capacitors that are fixedly connected in series,

an operational amplifier for producing said output signal from an output terminal thereof, having a third capacitor fixedly connected between ~~an~~said output terminal and a non-inverting input terminal of said operational amplifier, with said input signal being applied between an input terminal of said low-pass filter and said non-inverting input terminal,

first and second pluralities of switching elements operable for establishing a plurality of respectively different connection conditions between said first, second and third capacitors and said input terminal of the low-pass filter, said non-inverting input terminal and said inverting input terminal of said operational amplifier, and said output terminal of said operational amplifier, and

switching control means for selectively setting all of said first plurality of switching elements in a conducting state and in a non-conducting state and for selectively setting all of said second plurality of switching elements in a conducting state and in a non-conducting state, to establish said different connection conditions in a predetermined sequence,

said switching control means periodically controlling said switching elements to sequentially establish

during a first time interval, a condition in which said first capacitor is charged to a voltage of said input signal, while said second capacitor is discharged to zero and a charge of said third capacitor is left unchanged,

during a second time interval, a condition in which no charging or discharging of said first, second or third capacitors occurs,

during a third time interval, a condition in which said second and third capacitors are connected in parallel between said output terminal and inverting input terminal of said operational amplifier and are each charged from said first capacitor, causing a corresponding change in voltage across said third capacitor and a resultant change in output signal voltage from said operational amplifier, while said first capacitor is discharged to zero, and

during a fourth time interval, a condition in which no charging or discharging of said first, second or third capacitors occurs;

wherein said switching control means is configured to establish ~~as short~~ a duration ~~as possible~~ for said second time interval~~, within a range of durations whereby none of said first plurality of switching elements can enter said conducting status concurrently with any of said second plurality of switching elements~~ at a value whereby a decrease of stored charge in said first capacitor occurring within said interval, is predetermined to be substantially equal to a maximum permissible amount of error of DC gain of said low-pass filter, with said error being no greater than 3 percent of a predetermined value of said DC gain.

7. (Currently amended) A semiconductor pressure sensor apparatus comprising:

a semiconductor substrate having a region thereof formed to be thinner than surrounding regions to thereby constitute a diaphragm,

a first pair of piezoresistive elements mounted on said diaphragm, each adapted to exhibit an increase in resistance when pressure is applied to said diaphragm,

a second pair of piezoresistive elements mounted on said diaphragm, each adapted to exhibit a decrease in resistance when pressure is applied to said diaphragm, said piezoresistive elements being connected as an electrical bridge circuit, having a first connection point that connects a first one of said first pair of piezoresistive elements to a first one of said second pair of piezoresistive elements, a second connection point that connects a second one of said first pair of piezoresistive elements to a second one of said second pair of piezoresistive elements, a third connection point that connects said first one of said first pair of piezoresistive elements to said second one of said second pair of piezoresistive elements, and a fourth connection point that connects said second one of said first pair of piezoresistive elements to said first one of said second pair of piezoresistive elements,

a source of an electric current that is passed between said first and second connection points, and

a differential amplifier for amplifying a voltage difference between said second and third connection points;

wherein

an amplified output signal voltage produced from said differential amplifier is supplied to a low-pass filter as claimed in claim 1, for thereby detecting variations in pressure applied to said diaphragm.